Dense High Speed Digital Circuitry

The Challenge

A developer of space flight printed circuit board assemblies (PCBAs) which were Class IIIA products and had to meet NASA requirements, had a circuit packaging challenge. Class IIIA PCBAs must have designed feature sizes that meet defined manufacturing processes. The circuit density created power distribution challenges. The operating environment also created thermal challenges. Several layout firms had attempted to develop a packaging solution that solved the packaging challenges using smaller feature sizes. This compromised the Class IIIA manufacturability requirements.

The Process

The design team at San Diego PCB as IPC CID+ designers understand correct-by-construction parameters with Class IIIA requirements and immediately established a solution that meets manufacturing, performance and solved this dense layout.

The Solution

The team was able to design the PCBA layout in compliance with the Class IIIA manufacturability requirements. They guaranteed electrical integrity by ensuring an uninterrupted ground path to every signal and power rail. To aid in power integrity and enhance power delivery, a space-approved DuPont buried capacitance layer was added high in the stackup. This was verified by means of Hyperlynx simulation. The final product was approved and is working in space today.

RF Circuitry

The Challenge

A manufacturer of cellular RF-related products needed a layout team experienced with cellular RF products. There were both business and technical challenges. On the business side, there was a desire to keep products as low cost as possible and the prototype cycle was typically six weeks long. However, the technical challenges tend to drive up development costs so the company had initially selected an offshore layout firm.

Every micron of metal in an RF circuit has the potential to enhance or degrade transmission lines in an RF circuit. Most of the printed circuit board assemblies (PCBAs) have high speed digital circuitry adjacent to RF circuitry, creating the need to carefully manage the relational aspects of these two distinct types of circuitry to ensure highest performance. An additional challenge that was exacerbated by the short prototype cycle is that cellular RF operates on many bandwidths with multiple frequencies. This element of nuance-control, makes it critical to work iteratively with the RF engineer. While working offshore was one-third the cost of an onshore solution, language issues and technical misunderstandings were making the layout process take three times as long.

The Process

San Diego PCB's team had experience with cellular RF and understood the need to become the hands of the engineer in terms of translating the functionality he/she is designing into a workable layout. San Diego PCB's understanding of electromagnetic interference (EMI) theory helped make that level of coordination possible.

The team changed the strategy from a serial design process to a concurrent engineering, gated development process that compartmentalized digital and RF elements to allow for a parallel

development. The team also worked with the customer's manufacturer to ensure manufacturability considerations were incorporated in the layout process.

The Result

The customer established a long term relationship with San Diego PCB and as the teams established a close working relationship, the process became extremely efficient. Today, the team delivers layout in a third of time the offshore team took and is near the offshore team's original projected cost.